Design of Low-Power Analog Drivers Based on Slew-Rate Enhancement Circuits for CMOS Low-Dropout Regulators

Hoi Lee, *Member, IEEE*, Philip K. T. Mok, *Senior Member, IEEE*, and Ka Nang Leung, *Member, IEEE*

***Abstract*—Low-power analog driver based on a single-stage amplifier with an embedded current-detection slew-rate enhancement (SRE) circuit is presented. By developing a systematic way to design both the response time and optimal sizing of driving transistors in the SRE circuit, the SRE circuit can be controlled to turn on or turn off properly. In addition, the analog driver only dissipates low static power and its transient responses are significantly improved without transient overshoot when driving large capacitive loads. Implemented in a 0.6-μm CMOS process, a current-mirror amplifier with the current-detection SRE circuit has achieved over 43 times improvement in both slew rate and 1% settling time when driving a 470-pF load capacitor. When the proposed analog driver is employed in a 50-mA CMOS low-dropout regulator (LDO), the resultant load transient response of the LDO has 2-fold improvement for the maximum load-current change, while the total quiescent current is only increased by less than 3%.**

***Index Terms*—Amplifiers, analog driver, low-dropout regulator (LDO), slew rate, slew-rate enhancement (SRE) circuit, transient responses.**

I. Introduction

In RECENT years, low-dropout linear regulators (LDOs) are widely used in the portable battery-powered electronic devices as LDOs can convert decaying battery voltages to low-noise and accurate voltages for noise-sensitive systems. Since integrated CMOS LDOs only occupy small chip area, they are also adopted to power up sub-blocks of a system individually in the system-on-a-chip designs in order to tackle the crosstalk problem [1]. Both board space and external pins can be minimized. The design of high-performance CMOS LDO is thus necessary.

In LDO design, large gate capacitance of power transistor degrades the loop-gain bandwidth and the slew rate at the gate drive of the LDO in low-power condition [2], [3]. Both low quiescent current and fast load transient response, therefore, cannot be achieved simultaneously by using the generic LDO structure. To address this problem, a voltage buffer/driver can be inserted between the error amplifier and the power transistor. The voltage buffer should improve both the loop-gain bandwidth and slew rate at the gate drive of the power transistor, while the buffer dissipates small quiescent current in the static state [2], [4]. However, it is difficult to realize a good voltage buffer to meet the requirements perfectly in practice.

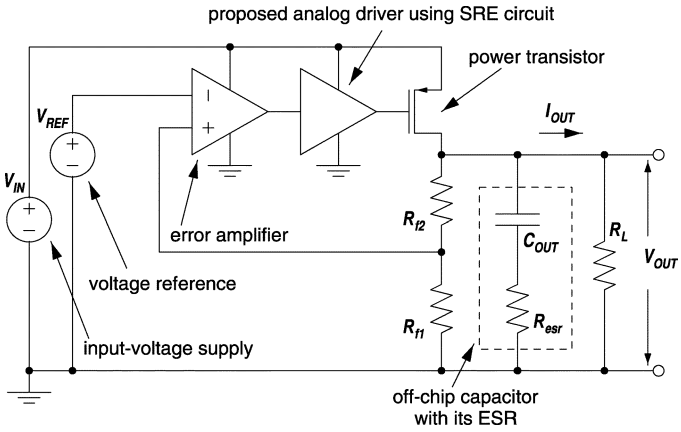

Fig. 1. Structure of LDO with the proposed analog driver.

This paper presents a new current-efficient analog driver for the CMOS LDO. The proposed analog driver is implemented by a single-stage amplifier (core amplifier) in noninverting unity-gain configuration with an embedded slew-rate enhancement (SRE) circuit as shown in Fig. 1. The paper is organized as follows. Section II addresses the design considerations of the proposed analog driver. Operating principle, systematic design method and circuit implementation of the current-detection SRE are discussed in Section III. Results of the analog driver and its application to LDO are shown in Section IV to justify the functionality of the proposed analog driver. Finally, conclusions are given in Section V.

II. Design Considerations of Proposed Analog Driver

In the analog driver, the open-loop low-frequency gain of the core amplifier is over 70 dB. With the unity-gain feedback configuration, the output resistance of the analog driver is reduced by its open-loop gain. The parasitic pole at the gate drive of the power transistor is then shifted to a higher frequency, thereby improving the loop-gain bandwidth of the LDO. The load-transient response of the LDO is originally limited by the slew rate at the gate drive of the power transistor, which is now improved by the embedded SRE circuit in the proposed analog driver. The SRE circuit only provides the dynamic current to charge and

Manuscript received May 10, 2004; revised November 26, 2004. This work was supported by the Research Grant Council of Hong Kong SAR Government under Project HKUST6150/03E. This paper was recommended by Associate Editor T. Saito.

H. Lee was with the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Hong Kong. He is now with Department of Electrical Engineering, University of Texas at Dallas, Richardson, TX 75083-0688 USA (e-mail: hoilee@utdallas.edu).

P. K. T. Mok and K. N. Leung are with the Department of Electrical and Electronic Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: eemok@ee.ust.hk; eealeung@ee.ust.hk).

Digital Object Identifier 10.1109/TCSII.2005.850781

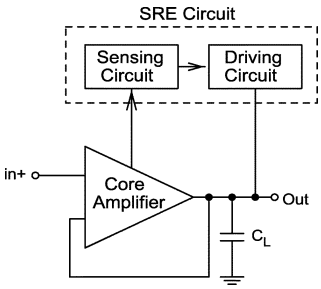

Fig. 2. Conceptual block diagram of the analog driver.

discharge the gate capacitance of the power transistor during transient, and is completely turned off in the static state. Consequently, the quiescent current of the analog driver is minimized, while the slew rate at the gate drive can still be enhanced. In short, the load-transient response and amount of quiescent-current dissipation of the LDO are determined by the performance of the SRE circuit.

The SRE circuit consists of a sensing and driving circuit. From the previous research work, different SRE circuits have been developed based on different sensing and driving circuits [5]–[9]. However, larger loading capacitance due to the additional structures and high dynamic current at input stage are problems in the existing methods. Therefore, a current-detection SRE circuit is adopted in the proposed analog driver [11]. Fig. 2 shows the conceptual block diagram of the analog driver with the current-detection SRE circuit. Structurally, the SRE circuit is connected in parallel to the core amplifier and serves as a plug-in module. The proposed concept is similar to that of the slew-rate dependent boost circuit in [12]. In the proposed circuit, the sensing circuit detects the changes in the current signal at the active load of the core amplifier such that the sensing circuit does not increase the loading of the error amplifier in the LDO. The driving circuit of the SRE circuit only applies the dynamic transient current to the output of the core amplifier to enhance the design flexibility of the core amplifier. The driving circuit also does not consume any static current. In addition, the implementation of the proposed SRE circuit has better gate-drive capability of the power transistor than that of [12] at low supply voltage if no low-threshold devices and forward bulk-biasing scheme are adopted. The detailed operating principle of the current-detection SRE is presented in Section III. Systematic ways to design the response time for turning on and turning off the driving circuit, and the optimal sizing of the drive transistors for supplying sufficient dynamic current to the gate drive of the power transistor will also be developed to maximize the dynamic current for improving the load-transient response of the LDO.

III. Current-Detection SRE Circuits

A. Principle of Operation

Fig. 3 shows the current-detection SRE circuit for the current-mirror amplifier, in which transistors $Ma1$ and $Ma2$ represent the active load of the current-mirror amplifier, $Md1$–$Md3$ are sensing transistors, and transistors $Md4$-$Md6$, Mp and Mn form the driving circuit. In particular, $Md4$, $Md5$, and Mp are

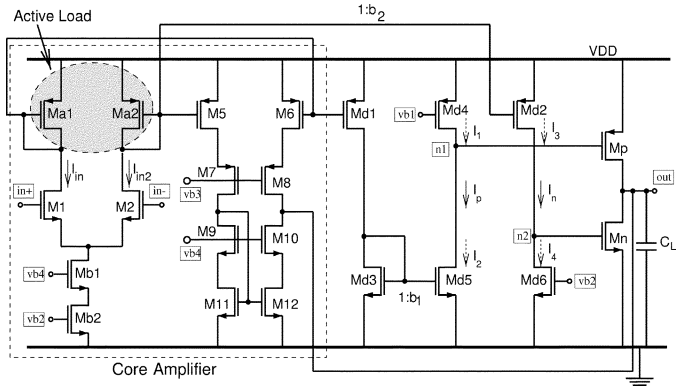

Fig. 3. Circuit diagram of the SRE circuit used in the current-mirror amplifier.

responsible for charging the capacitive load while $Md2$, $Md6$, and Mn are responsible for discharging the load.

In the static state, transistors $Md4$ and $Md5$ ($Md2$ and $Md6$) are designed such that if both transistors operate in the saturation region, their drain currents equal to I_1 and I_2 (I_3 and I_4), respectively, and $I_2 < I_1$ ($I_3 < I_4$). The dc current I_p and I_n is given by

$$I_p \approx I_2 \text{ and } I_n \approx I_3. \tag{1}$$

From (1), $Md4$ ($Md6$) operates in the triode region such that the voltage at node $n1(n2)$ is pulled up (down) to the positive (negative) supply voltage. Both drive transistors Mp and Mn are off.

When the amplifier is connected in unity-gain feedback configuration, a positive input voltage step at the input of the main amplifier leads to an increase in I_{in} and I_2. When I_2 is greater than I_1, the voltage at node $n1$ decreases and causes Mp to be heavily turned on. As a result, a large dynamic current is produced to charge up the load capacitance. When the output voltage reaches approximately the final value, I_2 decreases and causes Mp to shut off. Similarly, the transistor Mn can be controlled to discharge the load capacitance during the negative slewing period.

B. Response Time of SRE Circuit

The response time of the SRE circuit is determined by the time required to turn on or turn off the drive transistors Mp and Mn when a signal is applied at the input of the main amplifier. It is noted that the minimum signal amplitude to trigger the SRE circuit is δV. During the positive (negative) output slewing, transistor $Md4$ ($Md6$) is in the saturation region and provides a constant current to discharge (charge) the parasitic capacitance $C_{p1}(C_{p2})$ at node $n1$ ($n2$) from the voltage of $V_{\text{DD}} - |V_{\text{ov},Md4}|(V_{\text{ov},Md6})$ to $V_{\text{DD}} - |V_{\text{th},Mp}|(V_{\text{th},Mn})$ in order to turn on Mp (Mn). Therefore, the response time $t_{\text{resp},p}$ and $t_{\text{resp},n}$ of the SRE circuit for positive and negative slewing periods is approximately given by

$$t_{\text{resp},p} = \frac{(|V_{\text{th},Mp}| - |V_{\text{ov},Md4}|)\, C_{p1}}{b_1 g_m \delta V} \quad \text{(for positive slewing)} \tag{2}$$

$$t_{\text{resp},n} = \frac{(V_{\text{th},Mn} - V_{\text{ov},Md6}) C_{p2}}{b_2 g_m \delta V} \quad \text{(for negative slewing)} \tag{3}$$

where g_m is the transconductance of the input differential pair of the main amplifier, $V_{\rm ov}$ is the overdrive voltage of MOS transistor, and b_1 and b_2 are transistor ratios given by

$$b_1 = \frac{\left(\frac{\rm W}{L}\right)_{Md5}}{\left(\frac{\rm W}{L}\right)_{Md3}} \quad \text{and} \quad b_2 = \frac{\left(\frac{\rm W}{L}\right)_{Md2}}{\left(\frac{\rm W}{L}\right)_{Ma2}}. \tag{4}$$

Equations (2) and (3) show that the response time increases with the value of C_{p1} and C_{p2}. Increasing the sizes of transistors Mp and Mn thus slows down the response time of the SRE circuit.

C. Optimal Sizing of Drive Transistors

The size of drive transistors Mp and Mn is critical for controlling the amount of dynamic currents to charge and discharge the load capacitance. These currents then directly affect the maximum attainable slew rate. For a given slew rate SR and a loading capacitor C_L, assume that: 1) both Mp and Mn are in saturation regions with constant dynamic current during the positive and negative output slewing periods, respectively and 2) the channel length modulation of Mp and Mn is neglected. It can be demonstrated that the lower bounds of the size of Mp and Mn are given by

$$\left(\frac{\rm W}{L}\right)_{L,Mp} = \frac{2 \cdot {\rm SR} \cdot C_L}{\mu_p C_{\rm ox}\left(V_{\rm DD} - V_{{\rm ov},Md5} - |V_{{\rm th},Mp}|\right)^2} \tag{5}$$

$$\left(\frac{\rm W}{L}\right)_{L,Mn} = \frac{2 \cdot {\rm SR} \cdot C_L}{\mu_n C_{\rm ox}\left(V_{\rm DD} - |V_{{\rm ov},Md2}| - V_{{\rm th},Mn}\right)^2}. \tag{6}$$

Equations (5) and (6) indicate that in order to increase the slew rate for a particular load capacitance, device size of driving transistors should be increased. However, if drive transistors are too large, then the increase in the parasitic capacitance at nodes $n1$ and $n2$ can degrade the response time of the SRE circuit implied by (2) and (3). The maximum value of the size of drive transistors must be found by taking both the response time and the slewing period of the SRE circuit into consideration. The slewing period is defined as the time required for the output voltage changing from the initial voltage level to 90% of the final output voltage level. The response time is then set to 10% of the slewing period in order to allow the SRE circuit to shut down properly and give a reasonable settling time of the amplifier. As the output voltage of the main amplifier is changing and drive transistors Mp and Mn can be in different operating regions during transient, the upper bound of the size of Mp and Mn is found to depend on the lowest voltage level V_{OL}, and the highest voltage level V_{OH} of the voltage step ΔV, where $\Delta V = V_{OH} - V_{OL}$.

Suppose $\Delta V = 1\ V$ with $V_{OL} = 1.3$ V and $V_{OH} = 2.3$ V, the transistor Mp then operates in the triode region during the positive slewing period, as the output voltage is V_O of the amplifier is $V_{OL} < V_O < V_{OH}$ and $V_{OL} > (V_{{\rm ov},Md5} + |V_{{\rm th},Mp}|)$. Therefore, the upper bound of the size of Mp is given by

$$\left(\frac{\rm W}{L}\right)_{U,Mp} \leq \frac{0.1 C_L b_1 g_m \delta V}{\mu_p C_{\rm ox} C_{p1} V_1 \left(|V_{{\rm th},Mp}| - |V_{{\rm ov},Md4}|\right)} \times \ln\left(\frac{V_{\rm DD} - V_{OL}}{V_{\rm DD} - V_{OL} - 0.9\Delta V}\left(1 + \frac{0.9\Delta V}{2V_1 + V_{OL} - V_{\rm DD}}\right)\right) \tag{7}$$

where $V_1 = V_{\rm DD} - V_{{\rm ov},Md5} - |V_{{\rm th},Mp}|$. During the negative slewing period, the transistor Mn will operate in the saturation region when $(V_{\rm DD} - |V_{{\rm ov},Md2}| - V_{{\rm th},Mn}) < V_O < V_{OH}$ and in the triode region when $V_{OL} < V_O < (V_{\rm DD} - |V_{{\rm ov},Md2}| - V_{{\rm th},Mn})$. Therefore, the upper bound of the size of Mn is given by

$$\left(\frac{\rm W}{L}\right)_{U,Mn} \leq \frac{0.2 C_L b_2 g_m \delta V}{\mu_n C_{\rm ox} C_{p2} V_2 (V_{{\rm th},Mn} - V_{{\rm ov},Md6})} \times \left(\frac{V_{OH} - V_2}{V_2} + \frac{1}{2}\ln\left(\frac{2V_2}{V_{OL} + 0.1\Delta V} - 1\right)\right) \tag{8}$$

where $V_2 = V_{\rm DD} - |V_{{\rm ov},Md2}| - V_{{\rm th},Mn}$. The detailed derivations of (7) and (8) are described in the Appendix. The same derivation method given in the Appendix can be used to design different $(W/L)_{U,Mp}$ and $(W/L)_{U,Mn}$ for different values of ΔV, V_{OL} and V_{OH}. Based on (5)–(8), the optimal size of drive transistors Mp and Mn should be set within the range given by

$$\left(\frac{\rm W}{L}\right)_{L,Mp} \leq \left(\frac{\rm W}{L}\right)_{{\rm opt},Mp} \leq \left(\frac{\rm W}{L}\right)_{U,Mp} \tag{9}$$

$$\left(\frac{\rm W}{L}\right)_{L,Mn} \leq \left(\frac{\rm W}{L}\right)_{{\rm opt},Mn} \leq \left(\frac{\rm W}{L}\right)_{U,Mn.} \tag{10}$$

D. Simulation Results

Simulation using Bsim3v3 model of AMS (Austria Miko Systeme International AG, Austria) 0.6-μm CMOS process have been carried out to verify the functionality of the current-detection SRE circuit. The circuit schematic of analog driver is shown in Fig. 3 in which all biasing voltages of the amplifier are generated by wide-swing cascode current mirrors [13]. Fig. 4 shows the simulation results of ac responses of the core amplifier with and without the current-detection SRE circuit driving a load capacitance of 470 pF. Since poles and zeros from the analog driver potentially degrade LDO stability, small transistor sizes are used in the analog driver to minimize parasitic capacitances that generate parasitic poles and zeros. As both drive transistors Mp and Mn are off in the overall amplifier during the static state, there is almost no difference between the ac responses of the amplifier with and without the SRE circuit. It is confirmed that the SRE circuit does not affect the ac responses of the core amplifier.

IV. Results and Discussions

Implemented in AMS 0.6-μm CMOS process, the micrograph of the current-mirror amplifier with the current-detection SRE circuit is shown in Fig. 5. The SRE circuit occupies less than 25% of the total chip area of amplifier.

The measurements on small-signal ac responses and large-signal transient responses of the overall amplifier have been carried out by loading the output of the amplifier with load capacitance of 470 pF and 1 nF. The transient responses have been measured when the overall amplifier is in the unity gain noninverting configuration to test the functionality of the analog driver. The measured transient responses of the overall amplifier shown in Fig. 6 indicate that the amplifier does not have significant transient overshoot even if the load

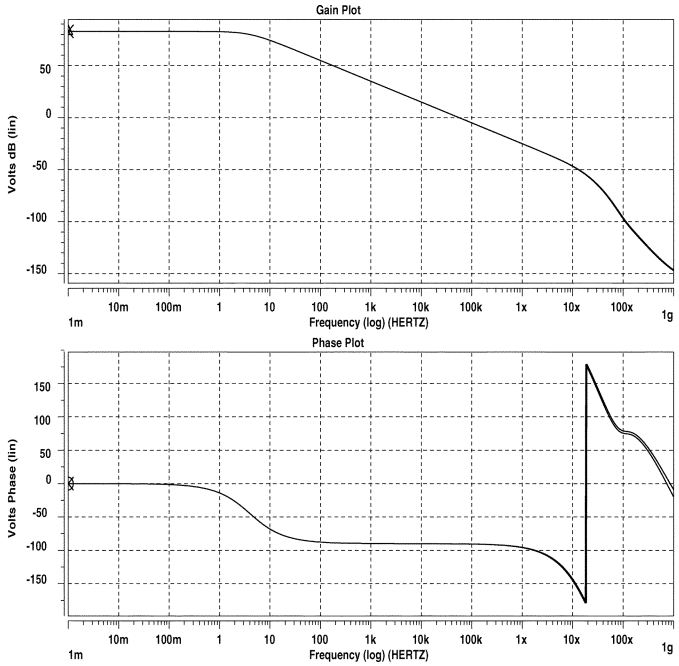

Fig. 4. Small-signal ac responses of the current-mirror amplifier with and without the current-detection SRE circuit in the static state.

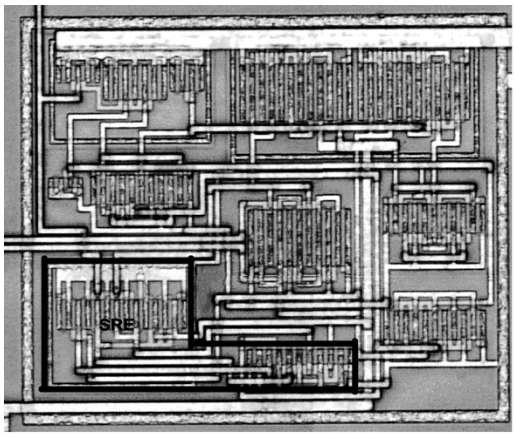

Fig. 5. Micrograph of the current-mirror amplifier with the SRE circuit.

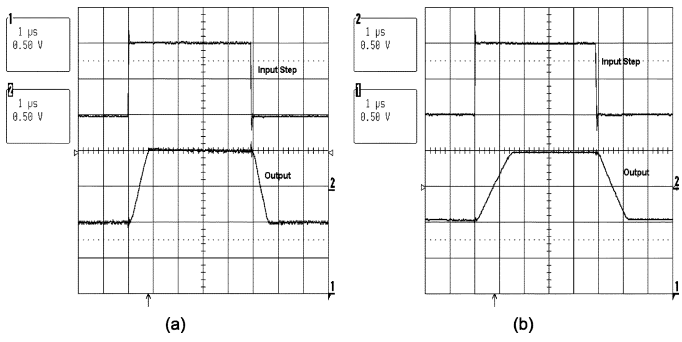

Fig. 6. Transient responses of the current-mirror amplifier with the SRE circuit when driving (a) a 470-pF load and (b) a 1-nF load with 1-V voltage step.

capacitance is changed by more than two times. This implies that the SRE circuit in the current-mirror amplifier is properly shut down before the end of the slewing periods. This justifies the sizing conditions of drive transistors Mp and Mn shown in (9) and (10). The detailed performance of the overall amplifier is summarized in Table I.

TABLE I
SUMMARY OF SIMULATION AND MEASUREMENT RESULTS

	Current-Mirror Amp. without SRE*	**Current-Mirror Amp. with SRE**
Static Power (mW)	0.22	**0.28**
Gain@10Hz	74 dB	**73 dB**
GBW	56 kHz	**57 kHz**
Phase Margin	89.7°	**90°**
SR+/SR- (V/μs)	0.037/0.0368 (C_L=470pF) 0.017/0.017 (C_L=1nF)	**1.5/1.73** (C_L=470pF) **0.7/0.81** (C_L=1nF)
Ts+/Ts- (1%) (μs)	31.3/31.4 (C_L=470pF) 66.7/66.7 (C_L=1nF)	**0.79/0.61** (C_L=470pF) **1.44/1.09** (C_L=1nF)
Area (mm^2)	N.A.	**0.027**
Supply Voltage	3 V	
Loading capacitor	1 MΩ // 470 pF	

Note:

1) Slew rate and 1% settling time were measured in unity-gain noninverting configuration with a 1-V step input.
2) * indicates simulation results.

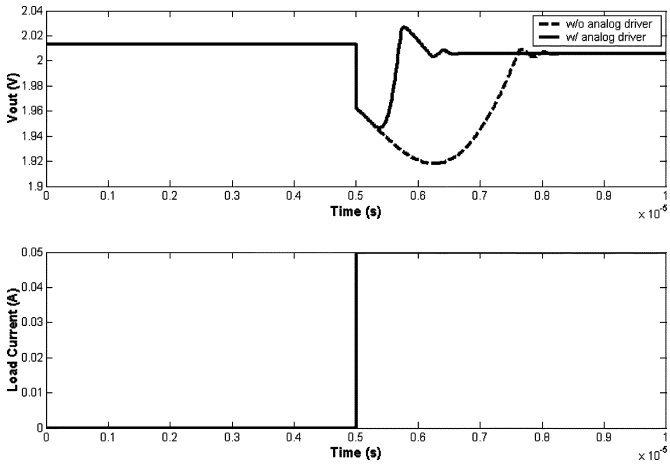

Fig. 7. Results of load-transient responses of the LDO with and without the proposed analog driver.

Comparing the performance of amplifiers with and without the SRE circuit driving a 470-pF load based on data in Table I, the average slew rate of the current-mirror amplifier shows improvement by 43 times and 1% settling time by 44 times when the SRE circuit is used. The SRE circuit only consumes 27.3% additional static current. Therefore, with the use of current-detection SRE circuit in the core amplifier, significant improvement in transient responses can be achieved in low-power condition.

When the overall amplifier is served as the analog driver and then adopted to the LDO according to the structure of Fig. 1, the load-transient response of the LDO is improved by 2.3 times with 50 mA output-current change as shown in Fig. 7. The static current of the LDO with the analog driver is only increased by less than 3%. The improvement of the load-transient response of the LDO is mainly due to the extra dynamic current provided by the proposed SRE circuit to reduce the output-voltage excursion during transient. In addition, the pole located at the output of the proposed analog driver will be shifted to a higher frequency due to the turn on of either drive transistor Mp or Mn during

transient, thereby improving the bandwidth of the LDO. It is thus verified that the proper design of the current-detection SRE circuit can enhance the load transient response of the LDO in low-quiescent-current condition.

V. Conclusion

This paper addresses the design of a low-power analog driver implemented by the current-mirror amplifier with a current-detection SRE circuit. Systematic design techniques of the SRE circuit are discussed to ensure that the driving transistors provide sufficient dynamic current to charge the load capacitance during transient and to shut off in the static state. The static current consumption of the analog driver can thus be minimized. The SRE circuit also does not affect the ac responses of the core amplifier due to its plug-in feature. When the current-mirror amplifier with the SRE circuit is utilized as the analog driver in the LDO, the load-transient response of the LDO achieves 2-fold improvement with less than 3% increase in the current consumption. Therefore, the proposed analog driver using the current-detection SRE circuit is effective in driving large capacitive loads under low-power condition. The proposed analog driver can also extend to other large-capacitive-load applications such as column buffers in flat-panel displays and switched-capacitor power converters for performance enhancements.

Appendix

This appendix provides the detailed derivations of (7) and (8) shown in Section III-C. The derivations are based on the particular example: $\Delta V = 1$ V, $V_{OL} = 1.3$ V and $V_{OH} = 2.3$ V.

As indicated in Section III-C, the transistor Mp always operates in the triode region during the positive output slewing period. The slewing period, $t_{\mathrm{slew},p}$ is determined by the time required to charge the loading capacitor with the output voltage changing from $V_o = V_{OL}$ to $V_o = 0.9\Delta V + V_{OL}$. Then, $t_{\mathrm{slew},p}$ is given by

$$\begin{aligned} t_{\mathrm{slew},p} &= \int_{V_{OL}}^{0.9\Delta V+V_{OL}} \frac{2C_L \mathrm{dV}_o}{\mu_p C_{\mathrm{ox}}\left(\frac{\mathrm{W}}{L}\right)_{\mathrm{Mp}}[2V_1(V_{\mathrm{DD}}-V_o)-(V_{\mathrm{DD}}-V_o)^2]} \\ &= \frac{C_L}{\mu_p C_{\mathrm{ox}}\left(\frac{\mathrm{W}}{L}\right)_{\mathrm{Mp}} V_1} \\ &\quad \times \ln\left(\frac{V_{\mathrm{DD}}-V_{OL}}{V_{\mathrm{DD}}-V_{OL}-0.9\Delta V}\left(1+\frac{0.9\Delta V}{2V_1+V_{OL}-V_{\mathrm{DD}}}\right)\right) \end{aligned} \quad (11)$$

where $V_1 = V_{\mathrm{DD}} - V_{\mathrm{ov},Md5} - |V_{\mathrm{tp}}|$. In addition, the response time of Mp is related to the slewing period by

$$t_{\mathrm{resp},p} \le 0.1 \cdot t_{\mathrm{slew},p}. \quad (12)$$

By substituting (2) and (11) into (12), the upper bound of the size of Mp can be found and is given in (7).

During the negative output slewing period, the transistor operates in the saturation region when $V_2 < V_o < V_{OH}$ and $V_2 = V_{\mathrm{DD}} - |V_{\mathrm{ov},Md2}| - V_{\mathrm{th},Mn}$, and in the triode region when $V_{OL} < V_o < V_2$. The slewing period of Mn, $t_{\mathrm{slew},n}$, can thus be considered to be the time required to discharge the load capacitance from $V_o = V_{OH}$ to $V_o = 0.1\Delta V + V_{OL}$ and is given by

$$\begin{aligned} t_{\mathrm{slew},n} &= \frac{2C_L}{\mu_n C_{\mathrm{ox}}\left(\frac{\mathrm{W}}{L}\right)_{\mathrm{Mn}}}\left(-\int_{V_{OH}}^{V_2}\frac{\mathrm{dV}_o}{V_2^2} - \int_{0.1\Delta V+V_{OL}}^{V_2}\frac{\mathrm{dV}_o}{2V_2V_o-V_o^2}\right) \\ &= \frac{C_L}{\mu_n C_{\mathrm{ox}}\left(\frac{\mathrm{W}}{L}\right)_{\mathrm{Mn}}}\left(\frac{2(V_{OH}-V_2)}{V_2}+\ln\left(\frac{2V_2}{0.1\Delta V+V_{OL}}-1\right)\right) \end{aligned} \quad (13)$$

where $V_2 = V_{\mathrm{DD}} - |V_{\mathrm{ov},Md2}| - V_{\mathrm{tn}}$. In addition, the response time of Mn is related to the slewing period by

$$t_{\mathrm{resp},n} \le 0.1 \cdot t_{\mathrm{slew},n}. \quad (14)$$

By substituting (3) and (13) into (14), the upper bound of the size of Mn is found and given by (8).

References

[1] D. D. Buss, "Technology in the Internet age," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, Feb. 2002, pp. 18–21.

[2] G. A. Rincon-Mora and P. E. Allen, "A low-voltage, low quiescent current, low drop-out regulator," *IEEE J. Solid-State Circuits*, vol. 33, no. 1, pp. 36–44, Jan. 1998.

[3] K. N. Leung and P. K. T. Mok, "A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pp. 1691–1702, Oct. 2003.

[4] S. K. Lau, K. N. Leung, and P. K. T. Mok, "Analysis of low-dropout regulator topologies for low-voltage regulation," in *Proc. IEEE Conf. Electron Devices and Solid-State Circuits*, Hong Kong, Dec. 2003, pp. 379–382.

[5] J. Ramírez-Angulo, "A novel slew-rate enhancement technique for one stage operational amplifiers," in *Proc. IEEE Midwest Symp. Circuits and Systems*, Ames, IA, Aug. 1996, pp. 11–13.

[6] R. Klinke, B. J. Hosticka, and H. J. Pfleiderer, "A very-high-slew-rate CMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. 24, no. 6, pp. 744–746, Jun. 1989.

[7] K. S. Yoon, "A CMOS digitally programmable slew-rate operational amplifier," *IEEE Trans. Circuits Syst. II, Analog. Digit. Signal Process.*, vol. 42, no. 11, pp. 738–741, Nov. 1995.

[8] M. G. Degrauwe, J. Rijmenants, E. A. Vittoz, and J. J. D. Man, "Adaptive biasing CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. SC-17, no. 6, pp. 522–528, Jun. 1982.

[9] K. Nagaraj, "CMOS amplifiers incorporating a novel slew rate enhancement circuit," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1990, pp. 11.6.1–11.6.5.

[10] S. Baswa, A. J. López-Martín, R. G. Carvajal, and J. Ramírez-Angulo, "Low-voltage power-efficient adaptive biasing for CMOS amplifiers and buffers," *Electron. Lett.*, vol. 40, no. 4, pp. 217–219, Feb. 2004.

[11] H. Lee and P. K. T. Mok, "A CMOS current-mirror amplifier with compact slew rate enhancement circuit for large capacitive load applications," in *Proc. IEEE Int. Symp. Circuits and Systems*, vol. I, 2001, pp. 220–223.

[12] G. A. Rincón-Mora, "Current-efficient low-voltage low dropout regulators," Ph.D. dissertation, Georgia Institute of Technology, Atlanta, 1996.

[13] D. A. Johns and K. Martin, *Analog Integrated Circuit Design*. New York: Wiley, 1997.